CLAIMS

What is claimed is:

1. A decision feedback equalizer (DFE) for processing a data signal and exhibiting concurrent soft and hard decision directed (dd) operating modes for providing respective soft dd and hard dd equalizer outputs, wherein each equalizer output symbol soft decision bit representation concurrently includes both hard and soft decision representations.

2. A decision feedback equalizer (DFE) for processing a data signal and exhibiting concurrent soft and hard decision directed (dd) operating modes for providing respective soft dd and hard dd equalizer outputs, wherein for each equalizer output symbol, a subset of its soft decision output bit representation corresponds to its hard decision bit representation.

3. A decision feedback equalizer (DFE) for processing a data signal and providing DFE output signals, said DFE comprising:

a feedforward filter (FFF) (10);

a feedback filter (FBF) (14);

a slicer (16), said slicer (16), said FFF (10) and said FBF (14) being mutually coupled for forming a decision feedback equalizer configuration, said equalizer configuration exhibiting concurrent hard and soft decision directed (dd) operating modes; and

wherein the DFE output bit representations corresponding to both said hard and soft dd operating modes are outputted concurrently.

4. A decision feedback equalizer (DFE) as recited in claim 3, including:

a controllable multiplexer (MUX) (22) coupled to said equalizer configuration for coupling a selected one of said outputs of said DFE to the input of said slicer (16), according to the value of a selector input to said MUX (22).

5. A decision feedback equalizer (DFE) as recited in claim 3, wherein the bit representation for each output symbol in said DFE outputs includes as a subset thereof a bit representation of said output of said slicer.

6. A decision feedback equalizer (DFE) as recited in claim 5, wherein said bit representation for each output symbol in said DFE outputs is associated with the FBF (14) input in said soft dd mode and wherein said bit representation of said output of said slicer (16) is associated with the FBF (14) input in said hard dd mode.

7. A decision feedback equalizer as recited in claim 4, including a lock detector (20) coupled to said DFE concurrent outputs for providing a lock signal indicative of an equalizer convergence condition according to an equalizer convergence detection algorithm.

8. A decision feedback equalizer as recited in claim 3, wherein said equalizer configuration exhibits a selectable blind mode of operation.

9. A decision feedback equalizer as recited in claim 7, wherein said equalizer configuration exhibits a selectable blind mode of operation, and

said equalizer including a mode switch (18) responsive to said lock signal and being coupled to said lock detector output, MUX output, and to said slicer (16) for providing respective control signals for controlling the operating mode characteristics of said FFF (10) and said FBF (14) and for selecting said operating modes responsive to said lock signal.

10. A decision feedback equalizer as recited in claim 9, wherein said mode switch (18) comprises a lock detector (20) and provides control signals to said FFF (10) and said FBF (14) for causing selection from among said dd and said blind modes of operation based upon lock characteristics of said DFE output signal.

11. A decision feedback equalizer (DFE) for processing a data signal and providing DFE output signals in accordance with any of a hard decision directed (dd) mode, a soft dd mode, and a blind mode, said DFE comprising:

a feedforward filter (FFF) (10) having a control input, having an adaptation error input, having an input for receiving said data signal, and having an output;

a feedback filter (FBF) (14) having a control input, having an adaptation error input, having first and second data inputs, and having first and second outputs;

a multiplexer (MUX) (22) having control input, having first and second inputs, and having an output;

a first summing unit (13) having a first input coupled to said output of said FFF (10), having a second input coupled to said first output of said FBF (14), and having an output coupled to said first input of said MUX (22);

a second summing unit (15) having a first input coupled to said output of said first summing unit (13), having a second input coupled to said second output of said FBF (14), and having an output coupled to said second input of said MUX (22);

a slicer (16) having an input coupled to said output of said MUX (22) and having an output;

a lock detector (20) for monitoring an equalizer convergence condition and providing a lock signal indicative of a locked condition;

a mode switch (18) having a control input coupled to said output of said lock detector, a first input coupled to said MUX (22) output, a second input coupled to said slicer (16) output, and two outputs coupled to the FBF (14) inputs;

said mode switch (18) coupling the said slicer (16) output to said first input to said FBF (14); and

said mode switch (18) further comprising a third summing unit (24) having a first input coupled to said output of said slicer (16), having a second input coupled to said output of said MUX (22), and having an output coupled to said second input of said FBF (14).

12. A decision feedback equalizer (DFE) as recited in claim 11, wherein said output of said slicer (16) is coupled to said first input of said FBF (14) by way of a dividing unit (26).

13. A decision feedback equalizer (DFE) as recited in claim 12, wherein said dividing unit (26) divides by a predetermined number.

14. A decision feedback equalizer (DFE) as recited in claim 13, wherein said dividing unit (26) divides by 32.

15. A decision feedback equalizer (DFE) as recited in claim 14, wherein said dividing unit (26) divides by 32 by performing a 5-bit right-shift operation.

16. A decision feedback equalizer (DFE) as recited in claim 11, wherein said input of said lock detector (20) is coupled to at least one of said first and second outputs of said DFE.

17. A decision feedback equalizer (DFE) as recited in claim 11, wherein said mode switch (18) control input is coupled to said lock detector (20) output, at least one of said inputs of said MUX (22) and said output of said slicer (16).

18. A decision feedback equalizer (DFE) as recited in claim 17, wherein said mode switch (18) selects one or other of said hard decision directed (dd) mode, said soft dd mode, and said blind mode, depending upon said lock signal and signal characteristics.

19. A decision feedback equalizer (DFE) as recited in claim 11, wherein the bit representation for each output symbol in said DFE outputs includes as a subset thereof a bit representation of said output of said slicer.

20. A decision feedback equalizer as recited in claim 11, wherein said bit representation for each output symbol in said DFE outputs is associated with the FBF (14) input in said soft dd mode and wherein said bit representation of said output of said slicer is associated with the FBF (14) input in said hard dd mode.

21. A decision feedback equalizer (DFE) for processing a data signal and providing DFE output signals, said DFE comprising:

means (10) for feedforward filtering of said data signal;

means (14) for feedback filtering;

means (16) for signal slicing; and

means for coupling said means (10) for feedforward filtering, said means (14) for feedback filtering, and said means (16) for signal slicing for forming a DFE configuration exhibiting concurrent hard and soft decision directed (dd) operating modes and outputs; and

means for coupling an input of said means for feedback filtering FBF (14) to an output of said means (16) for signal slicing in said hard dd operating mode and coupling a further input of said means for feedback filtering to one of said DFE output signals in said soft dd operating mode such that the bit representation for

each output symbol in said DFE output includes as a subset thereof a bit representation of said output of said slicer.

22. A decision feedback equalizer as recited in claim 21, including means (22) for multiplexing signals between said means (10) for feedforward filtering, said means (14) for feedback filtering, and said means for signal slicing (16), so as to cause said DFE configuration to operate in a blind operating mode.

23. A decision feedback equalizer as recited in claim 22, including means (22) for multiplexing signals between said means (10) for feedforward filtering, said means (14) for feedback filtering, and said slicer means (16) for signal slicing, so as to cause said DFE configuration to operate in a selected one of said operating modes.

24. A decision feedback equalizer as recited in claim 22, including means (20) for monitoring the convergence state of said DFE configuration.

25. A decision feedback equalizer as recited in claim 24 including means (22) for multiplexing signals between said means (10) for feedforward filtering, said means (14) for feedback filtering, and said slicer means (16) for signal slicing so as to cause said DFE configuration to operate in a selected one of said operating modes in accordance with said state of convergence.

26. A method for decision feedback equalization for deriving more than one output data signal from a data input signal to be processed, said method comprising the steps of:

applying said data input signal to be processed to a feedforward filter (FFF) (10);

coupling a feedback filter (FBF) (14) and a slicer (16) to said FFF (10) for forming therewith a decision feedback equalizer (DFE) configuration exhibiting concurrent hard and soft decision directed (dd) operating modes and outputs; and

coupling an input of said FBF (14) to an output of said slicer (16) in said hard dd operating mode and coupling a further input of said FBF (14) to one of said DFE output signals in said soft dd operating mode such that the bit representation for each output symbol in said DFE output includes as a subset thereof a bit representation of said output of said slicer (16).

27. A method for decision feedback equalization as recited in claim 26, including the step of multiplexing signals between said FFF (10), said FBF (14), and said slicer (16) so as to cause said DFE configuration to operate in a blind operating mode.

28. A method for decision feedback equalization as recited in claim 27 including the step of multiplexing signals between said FFF (10), said FBF (14), and said slicer (16) so as to cause said DFE configuration to operate in a selected one of said operating modes.

29. A method for decision feedback equalization as recited in claim 27 including the step of monitoring the convergence state of said DFE configuration.

30. A method for decision feedback equalization as recited in claim 29, including the step of multiplexing signals between said FFF (10), said FBF (14), and said slicer (16) so as to cause said DFE configuration to operate in a selected one of said operating modes in accordance with said state of convergence.

31. A decision feedback equalizer (DFE) as recited in claim 11, wherein the DFE outputs satisfy the following equations:

$$Z_{0k} = U_k + Y_k$$
$$Z_{lk} = U_k + Y_k + V_k = Z_{0k} + V_k$$

where Z_{0k} is the output in hard dd mode, Z_{1k} is the output in soft dd and blind mode, Y_k is the output of the FFF (10) filter block and U_k and V_k satisfy the following equations:

$$U_k = (C_k{}^T * \bar{I}_k) << 5$$
$$V_k = C_k{}^T * \bar{E}_k$$

where C_k is the equalizer FBF (14) tap coefficient vector at time k, $(.)^T$ is the transpose operation, $\bar{I}_k$ and $\bar{E}_k$ are the corresponding vectors of the I_k and E_k variables, I_k is the first FBF (14) input and E_k is the second FBF (14) input.

32. A decision feedback equalizer (DFE) as recited in claim 31, wherein the equalizer FBF (14) tap adaptation in decision directed mode may satisfy one of the following equations:

$$C_{k+1} = C_k + \mu * Er_k * (\bar{I}_k << 5) \quad \text{or}$$

$$C_{k+1} = C_k + \mu * Er_k * ((\bar{I}_k << 5) + E_k) = C_k + \mu * Er_k * Z_k$$

where C_{k+1} is the equalizer FBF (14) tap coefficient vector at time k+1, C_k is the equalizer tap coefficient vector at time k, μ is the adaptation step size, <<5 means a left shift of 5 bits, or multiplication by 32, Zk is the MUX (22) output, $\bar{I}k$ and $\bar{E}k$ are the corresponding vectors of the Ik and Ek variables, Ik is the first FBF (14) input, Ek is the second FBF (14) input and Erk is the mode tap adaptation error; and

wherein the equalizer FBF tap adaptation in blind mode satisfies the second equation above.

33. A decision feedback equalizer (DFE) as recited in claim 31, wherein the MUX (22) selector output Z_k may be chosen to be one of Z_{0k} and Z_{1k} when in both hard and soft dd modes and is Z_{1k} when in blind mode.